#13 Appeal Brief J. McMillan 3/4/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Henry Haldane et al.
Serial No.: 09/614,794
Filed: July 12, 2000
For: ELECTRONIC COMPONENT AND METHOD OF MANUFACTURE

January 21, 2003

Art Unit: 2811
Examiner: D. Owens
Docket No.: SC11152ZP

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE AS FIRST CLASS MAIL IN AN ENVELOPE ADDRESSED TO: COMMISSIONER OF PATENTS AND TRADEMARKS WASHINGTON, D.C. 20231, ON: 1/2/03
MOTOROLA, INC.
Elaine Cox
SIGNATURE
DATE 1/21/03

APPELLANTS' BRIEF ON APPEAL

COMMISSIONER OF PATENTS AND TRADEMARKS
WASHINGTON, D.C. 20231

BOARD OF PATENT APPEALS & INTERFERENCES:

This brief is filed pursuant to 37 C.F.R. §1.192 in the matter of the Appeal to the Board of Appeals and Interferences of the rejection of the claims of the above-referenced application for patent. Please charge the filing fee of $320.00 (37 C.F.R. §1.17(c)) to Deposit Account 502117. This page is enclosed in triplicate for this purpose.

REAL PARTY IN INTEREST

The present application is wholly assigned to MOTOROLA, INC., a Delaware corporation with its headquarters in Schaumburg, Illinois.

RELATED APPEALS AND INTERFERENCES

Appellants are unaware of other appeals or interferences that will directly affect, be directly affected by, or have a bearing on the Board's decision in this appeal.

STATUS OF CLAIMS

Appellants originally filed claims 1-34 of the present application on July 12, 2000. A requirement to elect between the claims of Group 1 (claims 1-21 and 34) and Group II (claims 22-33) was mailed on December 4, 2001. Appellants responded by provisionally electing Group I (claims 1-21 and 34) without traverse on January 2, 2002. In an Office Action mailed March 15, 2002, claims 22-33 were withdrawn because the restriction requirement was made final. Also in this Office Action, the Examiner rejected claims 6 and 34 under 35 U.S.C. 112, second paragraph, claims 1-5, 7, 8, 10, 13, 14, 18, 20 and 21 over U.S. Patent 6, 268,262 by Loboda under 35 U.S.C. 102(e) and claims 9 and 19 over Loboda under 35 U.S.C. 103(a). In addition, the Examiner objected to claims 11, 12 and 15-17 as being dependent upon a rejected base claim. Appellants responded to the rejections in a communication mailed June 17, 2002 by amending claims 1, 6, 14, 15, 20, 21 and 34 and canceling claims 4 and 22-33 without prejudice. In an Office Action mailed August 23, 2002, the Examiner objected to the drawings under 37 CFR 1.83(a), rejected claims 14-21 and 34 under 35 U.S.C. 112, first paragraph, rejected claims 1-3, 5, 7, 8, 10 and 13 over

Loboda under 102(e), rejected claim 9 over Loboda under 35 U.S.C. 103(a), and objected to claims 11 and 12 as being dependent upon a rejected base claim. This rejection was made final. Appellants did not file a Response After Final Action pursuant to 37 C.F.R. §1.116. Instead, Appellants mailed a Notice of Appeal on November 22, 2002. This Appeal Brief is submitted in support of the Notice of Appeal.

STATUS OF AMENDMENTS

The claims being appealed are claims 1, 6, 14, 15, 20, 21 and 34 as amended in the communication mailed June 17, 2002 and claims 2-5, 7-13 and 16-19 as originally filed.

SUMMARY OF THE INVENTION

Appellants' invention relates generally to electronic components having airbridges. Airbridges are used in electronic components to increase their interconnect speed. Many prior art electronic components use airbridges made of gold to provide low electrical resistance, but gold is a soft material. The soft, exposed gold of the airbridge is often damaged during semiconductor wafer processing, assembly, and packaging in an automated manufacturing process. Thus, manual processing, which is expensive and time consuming, is undesirably used.

Appellants' invention relates to an airbridge having at least a first and second layer formed over a substrate, wherein the second layer is formed over the first layer. In a preferred embodiment, the second layer is a passivation layer that protects the airbridge during semiconductor wafer processing, assembly, and packaging.

A discussion of one embodiment forming an airbridge begins on page 4, line 20, of the present application. As illustrated in FIG. 3, a

sacrificial layer 240 is formed over a portion of a substrate 110 and a device 130. Described on page 6, beginning at line 10 and shown in FIG. 4, layer 460 and layer 450 are formed over the sacrificial layer 240 to form a portion of the airbridge. Next, a plating mask 555 as shown in FIG. 5 and taught on page 7, lines 7-16 is formed. An electrically conductive layer 660 is plated over layer 450 and the plating mask 555 is subsequently removed, as shown in FIG. 6 and described on page 7, line 18 to page 8, line 7. After removing the plating mask 555, the sacrificial layer 240 is removed to form a gap 770, as shown in FIG. 7 and as taught on page 8, line 8- 16. The (passivation) layer 880 is formed over layer 450 so that the airbridge 890 includes the layer 880, the layer 450 and the layer 460 as shown in FIG. 8 and described on page 8, starting at line 17.

Beginning on page 12, line 14, a description of the benefits and optimal properties of the layer 880 is described. For example, the layer 880 is preferably not located underneath a substantial portion of the airbridge to minimize the parasitic capacitance between the airbridge and the underlying interconnect layers.

ISSUES

1) Are the drawings patentable under 37 CFR 1.83(a)?
2) Are claims 14-21 and 34 supported by Appellants' original patent application as required under 35 U.S.C. §112, first paragraph?
3) Are claims 1-3, 5, 7, 8, 10 and 13 patentable over Loboda (U.S. 6,268,262) under 35 U.S.C. 102(e)?
4) Is claim 9 patentable over Loboda (U.S. 6,268,262) under 35 U.S.C. 103(a)?

GROUPING OF CLAIMS

The Appellants respectfully request that the appealed claims be considered according to the following division:

Group A--> Claims 14-21 and 34
Group B--> Claims 1-3, 5, 7, 8, 10 and 13
Group C--> Claim 9

The requested division is on the basis that the claims of Group A are directed to a semiconductor component that has a gap between a portion of the airbridge and a first electrically insulative layer and is rejected under 35 U.S.C. §112. Group B is directed to an electronic component where the thickness of the second layer is less than fifty percent of that of the first layer and the gap combined and is rejected under 35 U.S.C. §102(e) over Loboda (U.S. 6,268,262). Group C is directed to an electronic component having the second layer of an airbridge that has a compressive stress level of approximately 0 to 200 MegaPascals and is rejected over Loboda under 35 U.S.C. §103(a). Appellants submit that the claims of each group stand or fall together.

ARGUMENTS

Arguments with Respect to the Objection of the Drawings

The Examiner objects to the drawings under 37 CFR 1.83(a), which states that the "drawings...must show every feature of the invention specified in the claim." The Examiner contends that a gap between a portion of the airbridge and the first electrically insulative layer as stated in claims 14 and 22 is not shown. Appellants respectfully submit that the gap is shown as element 770 in FIG. 8.

(See page 8, line 8 of Appellants' specification.) As taught on page 4, lines 14-18 of the specification, an electrically insulative layer may be formed over the electrically conductive layer 120 and thus also over the semiconductor device 130. In other words, the semiconductor device 130 between the electrically conductive layer 120 may include an electrically insulative layer. The gap 770 in FIG. 8 is between the semiconductor device 130 that may include an electrically insulative layer at a top surface, as previously discussed, and the airbridge 890, which includes passivation layer 880, plating layer 660, and layer 450. Thus, FIG. 8 shows a gap between a portion of the airbridge and the first electrically insulative layer as stated in claims 14 and 22. For this reason, this objection should be withdrawn.

Arguments for Group A

Appellants submit that claims 14-21 and 34 are clearly supported by their original patent application, and thus claims 14-21 and 34 contain subject matter that is described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. The specific claim language alleged by the Examiner to be unsupported by Appellants' original patent application will now be discussed.

In the Office Action of August 23, 2002, the stated that Appellants "specification does not disclose a semiconductor device, wherein a gap exists between a portion of the airbridge and a first electrically insulative layer, as required in claims 14 and 20."

Appellants respectfully submit that their original patent specification clearly states on page 9, lines 8,

> "[t]urning to FIG. 7, the sacrificial layer [240] is removed to form a gap 770 underneath layer 660 and 450 between layer 450 and substrate 110"

and continues to state a process that can be used to remove the sacrificial layer 240. As stated on page 6, lines 10-12, "layer 450 located underneath layer 460 ...[is] a portion of an airbridge." As explained in regards to the objection of the drawings, on page 4, lines 14-19 an optional insulative layer can be formed over the electrically conductive layer 120 of FIG. 1. One of ordinary skill in the art acknowledges that by forming the optional insulative layer over the conductive layer 120, the optional insulative layer will inherently also be formed on the portion of the semiconductor substrate between the conductive layer 120 since no masking or selective deposition process is discussed. Therefore, when viewed as a whole the specification describes that a gap exists between a portion of the airbridge and a first electrically insulative layer. There is no requirement that the exact terminology used in a claim is in the specification. Instead, the claims only need to be supported by the specification and drawings. MPEP 2173.05(a). Thus, Appellants respectfully submit that the Examiner is in error.

In light of these arguments, Appellants respectfully submit that their original patent application contains a written description of the claimed invention, in that their disclosure reasonably conveys to one skilled in the art that they had possession of the claimed invention. Therefore, Appellants respectfully assert that the Examiner's rejection of claims 14-21 and 34 under 35 U.S.C. §112, first paragraph, is in error.

Furthermore, in rejecting claims under 35 U.S.C. §112, first paragraph, the Examiner bears the initial burden of presenting evidence or reasons why persons skilled in the art would not recognize in the disclosure a description of the invention defined by the claims (See *In re Gosteli*, 10 USPQ2d 1614, 1618 (CAFC 1989) which cites *In re Wertheim*, 191 USPQ 90, 97 (CCPA 1976)). However, if the disclosure allows one of ordinary skill in the art to recognize that the Appellants' invented what is claimed, then a rejection of the claims under 35 U.S.C. §112, first paragraph, is improper (See *In re Gosteli*, 10 USPQ2d 1614, 1618 (CAFC 1989)). In

view of the arguments discussed above, the Examiner has failed the initial burden of presenting evidence or reasons why persons skilled in the art would not recognize in the disclosure a description of the invention. Thus, the rejection should be withdrawn.

Arguments for Group B

The Examiner uses Loboda in the rejections of Group B under 35 U.S.C. 102(e). In regards to Loboda, Appellants respectfully submit that the claims of Groups B are not anticipated by the cited prior art. A reference is anticipatory only if it discloses all limitations of a claim. *Jamesbury Corp. v. Litton Indus. Products*, 756 F.2d 1556, 225 USPQ 253 (Fed. Cir. 1985); *Atlas Powder Co. v. du Pont*; 750 F.2d 1569, 224 USPQ 409 (Fed. Cir. 1984); *American Hospital Supply v. Travenol Labs*, 745 F.2d 1, 223 USPQ 577 (Fed. Cir. 1984). Appellants submit that Loboda does not teach all limitations of claims in Group B.

More specifically, Loboda fails to teach all limitations of independent claim 1. Loboda fails to teach that the second layer is less than a combined thickness of the first layer and the gap. (See lines 9-10 of claim 1 in the Appendix). The Examiner contends that Loboda teaches, "the thickness of the second layer is less than fifty percent of that of the first layer and the gap combined." The Examiner relies upon Loboda's figures to teach the dimensions because nowhere in the specification does Loboda teach this limitation because Loboda is silent as to the thickness of the second layer. The Examiner states that the drawings in combination with the specification can be relied upon for what they would reasonably teach one of ordinary skill in the art, which is correct. However, the Examiner expands on this concept and believes that because Loboda teaches that the second layer is a protective coating it implies a thin layer. Nowhere does Loboda teach or suggest that the second layer is thin. Furthermore, the Examiner fails to provide any support from any teachings that a protective coating implies a thin layer. While a protective coating *can* be a thin layer, Appellants disagree that a

protective coating *must* be a thin layer. For example, in U.S. 5,804,869 filed before the present application, a "relatively thick nitride or oxide passivation layer" is taught (Column 1, lines 66-67). A copy of the patent is attached for reference. The teaching of a passivation layer does not imply that the layer is relatively thin as it can be relatively thick. Thus, Loboda's passivation layer may be thick or thin and without any teaching or suggestion, one skilled in the art cannot presume the thickness of Loboda's passivation layer.

Furthermore, the Examiner states that not only is the second layer thin (which as discussed above is an incorrect interpretation of Loboda's second layer), based on the drawings the second layer is "very thin." In other words, the Examiner is relying on Loboda's figures to each that second layer is less than a combined thickness of the first layer and the gap. As stated in Appellants' amendment June 17, 2002 it is improper to on Loboda's figures to teach dimensional limitations because Loboda fails to state that the figures are drawn to scale and fails to teach any dimensions of the second layer in the specification. It is improper to rely upon the dimensions and proportions of features in figures if the figures are not drawn to scale. MPEP 2125 and *Hockerson-Halberstadt, Inc. v. Avia Group Intern., Inc., 55 USPQ2d 1487, (Fed Cir. 2000)* (*Hockerson-Halberstadt* cites *In re Wright, 569 F.2d 1124, 1127, 193 USPQ 332, 335 (CCPA 1977)* which states, "Absent any written description in the specification of quantitative values, arguments based on measurements of a drawing are of little value," and *In re Olson, 41 C.C.P.A. 871, 212 F.2d 590, 592, 101 USPQ 401, 402, (CCPA 1954).*) The inference the Examiner draws from Loboda's figures is, therefore, improper.

For at least these reasons, Loboda fails to teach or suggest all features of the claims of Group B. Reversal is respectfully requested.

Arguments for Group C

The Examiner rejects Group C under 35 U.S.C. 103(a) over Loboda. Appellants respectfully submit that the Examiner has failed to establish a prima facie case of obviousness, which is the burden of the USPTO when rejecting claims under 35 U.S.C. 103. *In re Reuter*, 651 F.2d 751, 210 USPQ 249 (CCPA 1981). The case of prima facie obviousness is not met because the references cited by the Examiner in support of the rejection do not teach all of the claim limitations and in addition, there is no motivation to alter Loboda as the Examiner suggests. *In re Royka*, 180 USPQ 580 (CCPA 1974); *In re Wilson*, 165 USPQ 494 (CCPA 1970); *In re Fine*, 5 USPQ2d 1596 (CAFC1988).

As a first point, the claim of Group C depends from independent claim 1 of Group B. As discussed in regards to Group B although the rejection of Group B is a novelty rejection, Loboda both fails to teach and suggest all limitations of claim 1 of Group B because the Examiner's reliance on Loboda's figures to teach the second layer is less than a combined thickness of the first layer and the gap is improper. For at least this reason, the claim of Group C is patentable over Loboda under 35 U.S.C. 103(a).

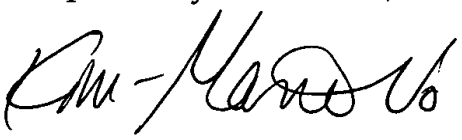
Additionally, even if Loboda taught or suggested all the limitations of claim 1 from which the claim of Group C depends, there is no teaching or suggestion from Loboda that the second layer of the airbridge has a compressive stress level of approximately 0 to 200 MegaPascals, as stated in claim 9 of Group C. (See lines 2-3 of claim 9 in the Appendix.) Loboda fails to teach the second layer having such a compression stress level. However, the Examiner contends that the compressive stress level is a function of thickness and that one skilled in the art would change the thickness of the layer to achieve such a stress level. As explained on page 9, lines 14-19 of Appellants' specification the desired compressive stress level is achieved by controlling the temperature and pressure of the deposition process. Loboda teaches that the deposition process used to form Loboda's second layer 13 is "non-critical" (Column 4, lines 41-48). Furthermore, Loboda fails to state any pressure ranges or

requirements for the deposition process for forming the second layer. Due to Loboda's lack of teaching or suggestion as to the pressure used, Loboda fails to suggest to one skilled in the art to experiment with the pressure. Since, as taught by Appellants' specification, temperature and pressure determine stress one skilled in the art would not be motivated based on Loboda to modify the parameters that would achieve the stress level stated in the claim of Group C.

In addition, Loboda fails to state or suggest altering or achieving stress of the second layer or any layer of the airbridge. There is no motivation to change the stress properties from Loboda or any cited prior art. Only Appellants' specification teaches such an idea. Using Appellant's specification as motivation to alter the prior art is improper.

For all the myriad of reasons above, claim 9 is patentable over Loboda under 35 U.S.C. 103(a). Withdrawal of the rejection is herein requested.

Respectfully submitted,



Kim-Marie Vo
Agent for Appellants
Reg. No. 50,714
Ph: (512) 996-6849

APPENDIX

1 An electronic component comprising:
a substrate; and
an airbridge located over the substrate and having at least a first layer and a second layer, wherein a first portion of the second layer is over the first layer,
wherein:
a gap exists between a portion of the airbridge and the substrate; and
a thickness of the second layer is less than a combined thickness of the first layer and the gap;
the airbridge is electrically conductive; and
the first layer of the airbridge is less resistive than the second layer of the airbridge.

2. The electronic component of claim 1 wherein:
the second layer is a passivation layer.

3. The electronic component of claim 1 wherein:
the second layer is harder than the first layer.

4. The electronic component of claim 1 wherein:
a gap exists between a portion of the airbridge and the substrate; and
a thickness of the second layer is less than a combined thickness of the first layer and the gap.

5. The electronic component of claim 4 wherein:
the thickness of the second layer is less than fifty percent of the combined thickness of the first layer and the gap.

6. The electronic component of claim 1 wherein:

a second portion of the second layer is located underneath an edge of the first layer.

7. The electronic component of claim 1 wherein:
the second layer is absent underneath a center portion of a width of the airbridge.

8. The electronic component of claim 1 wherein:
a gap exists underneath a portion of the airbridge; and
the gap is unsealed underneath the portion of the airbridge.

9. The electronic component of claim 1 wherein:
the second layer of the airbridge has a compressive stress level of approximately 0 to 200 MegaPascals.

10. The electronic component of claim 1 wherein:
the airbridge further comprises:
a third layer underneath the first layer; and
the third layer is more resistive than the first layer.

11. The electronic component of claim 10 wherein:
the second layer is more resistive than the third layer.

12. The electronic component of claim 1 wherein:
the second layer of the airbridge is electrically conductive.

13. The electronic component of claim 1 wherein:
the second layer of the airbridge is electrically insulative.

14. A semiconductor component comprising:
a semiconductor substrate;
a semiconductor device supported by the semiconductor substrate;

a first electrically insulative layer overlying the semiconductor substrate and the semiconductor device; and

an airbridge located over the semiconductor substrate, located over the first electrically insulative layer, and electrically coupled to the semiconductor device,

wherein:

a gap exists between a portion of the airbridge and the first electrically insulative layer;

the airbridge has a first electrically conductive layer; and

the airbridge has a second electrically insulative layer overlying the first electrically conductive layer.

15. The semiconductor component of claim 14 wherein:

the second electrically insulative layer is a passivation layer harder than the first electrically conductive layer; and

the airbridge further comprises:

an electrically conductive barrier layer located underneath the first electrically conductive layer and more resistive than the first electrically conductive layer.

16. The semiconductor component of claim 15 wherein:

a thickness of the second electrically insulative layer is less than fifty percent of a combined thickness of the electrically conductive barrier layer, the first electrically conductive layer, and the gap.

17. The semiconductor component of claim 15 wherein:

the second electrically insulative layer is devoid of sealing the gap underneath the portion of the airbridge.

18. The semiconductor component of claim 14 wherein:

the second electrically insulative layer is absent underneath a center portion of a width of the airbridge.

19. The semiconductor component of claim 14 wherein:
the second electrically insulative layer has a compressive stress level of approximately 100 MegaPascals.

20. A method of manufacturing an electronic component comprising:
providing a substrate;
forming an electrically insulative layer over the substrate;
forming a first layer over the first electrically insulative layer to form a first portion of an airbridge;
forming a first portion of a second layer over the first layer to form a second portion of the airbridge over the substrate,
wherein:
the airbridge is electrically conductive; and
the first layer of the airbridge is less resistive than the second layer of the airbridge; and
forming a gap between the airbridge and the electrically insulative layer.

21. The method of claim 20 further comprising:
forming a semiconductor device at least partially located within the substrate; and
wherein:
forming the first layer further comprises:
providing the first layer comprised of an electrically conductive material;
forming the second layer further comprises:
providing the second layer comprised of an electrically insulative material; and
forming the electrically insulative layer further comprises:
forming the electrically insulative layer over the semiconductor device.

34. The method of claim 20 further comprising:

designing the airbridge to have a design width,

wherein:

forming the first layer further comprises:

forming the first layer to have a first layer width greater than the design width; and

forming the second layer further comprises:

forming a second portion of the second layer underneath edges of the first layer; and

keeping the second layer absent underneath a central portion of the first layer, the central portion of the first layer having the design width.